Ayoosh Bansal

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Passionate about crafting innovative and efficient systems to overcome complex challenges, I strive to unravel intricacies and find elegantly simple solutions. My problem-solving methodology revolves around harnessing expertise across diverse layers within a system, fostering collaboration among components, and prioritizing simplicity in design. This approach has empowered me to architect frameworks for safe autonomous driving, enable comprehensive security auditing for real-time systems, and mitigate execution variability stemming from cache coherence mechanisms. I am excited to continue tackling new challenges and create innovative solutions that drive progress.

Education

University of Illinois Urbana-Champaign

PhD in Computer Science, , GPA 4/4, Advised by Prof. Lui Sha — Aug 2017 - Aug 2024 (Expected)

Dissertation title : Safe and Secure Autonomous Driving
Committee : Lui Sha (Chair), Marco Caccamo, Adam Bates, Parameswaran Ramanathan
Research Topics : Cyber-Physical Systems, Real-Time Systems, Functional Safety, Temporal Safety, System Security, Architecture

University of Wisconsin-Madison

Master of Science in Electrical Engineering, GPA 4/4 — Sep 2013 - May 2015

Birla Institute of Technology and Science Pilani, India

Bachelor of Engineering Electrical and Electronics, CGPA 8.6/10 — Aug 2006 - Jul 2010

Research Experience

Cyber Physical Systems Integration Lab, UIUC — Urbana

Graduate Research Assistant — Aug 2017 – Present

- Conducted diverse research within the realms of cyber-physical and real-time systems, enhancing functional safety, bolstering system security, and refining temporal predictability. A presentation summarizing the research works and publications is available here.
- Ongoing work on *Synergistic Simplex* system architecture that harnesses cooperation among safety- and mission-critical elements, as well as between perception and control modules, to enhance the safety and performance of autonomous ground and aerial vehicles.
- Devised *Perception Simplex*, a system architecture for autonomous vehicles that decouples mission and safety responsibilities, providing verifiable obstacle detection and deterministic collision avoidance within the operational design domain.
- Recognizing the lack of context-aware metrics for object detection in autonomous driving, created *Risk Ranked Recall*.
- Optimized security auditing for real-time applications, creating *Ellipsis*. Harnessing the inherent predictability of behaviors in real-time applications, *Ellipsis* all but eliminates the possibility of audit event loss during typical operation and significantly curtails auditing data volume (> 90%) while preserving security-relevant information.
- Introduced a new memory type, *Inner Non-Cacheable, Outer Cacheable*, empowering real-time applications to bypass cache coherence mechanisms and mitigate memory access latency variability selectively for shared data, with no impact on private data. Prototype implementation on Linux Kernel and Gem5 simulator, yielded 52% less worst-case latency and negligible impact on performance.
- Helped design security-aware task scheduling for real-time applications and input prioritization schemes for object detection DNN.

University of Wisconsin-Madison — Madison

Graduate Research Assistant — Sep 2014 – May 2015

- Conceptualized thermal capacity of computational systems, analogous to computational capacity. Devised software scheduling policies that ensure the processor core temperature can be kept below a threshold. Thermal capacity trivializes thermal aware scheduling complexity and can schedule both periodic and aperiodic tasks.
- Studied emerging distributed electricity markets and developed a Simulink and NS3 co-simulation framework for systems containing electrical and network elements.

Graduate Student — Sep 2013 – May 2014

- Developed software-assisted bias-free branch predictor, a compiler assisted improvement to history based branch predictors. Strongly biased branch instructions are marked by the compiler with branch direction. Marked branch instructions are predicted as marked and not entered in branch history. Reduced branch misprediction rate by 0.35% for SPEC CPU 2006 benchmarks on GEM5 simulator.
- Conducted an analysis of solid-state storage devices, focusing on compatibility with existing file systems and the consistency features of the drive to protect against loss of cached writes. Eliminating write batching improved varmail benchmark iops by 3.6%. Developed faster special case checksums using Deterministic Zero after Trim feature. Implemented as an improvement to Optimistic Crash Consistency file system, Improving iops by 4.1%.
- Implemented a configurable Neural Network Processing Unit (NPU) on a Virtex-5 FPGA, capable of accelerating different algorithms by running multilayer perceptron neural networks on the NPU.

Professional Experience

NVIDIA Santa Clara

Automotive System Software Intern May 2020 – Aug 2020

- Engineered a hypervisor-level latency analysis system aimed at optimizing applications with stringent latency requirements.

Automotive System Software Intern Jun 2018 – Aug 2018

- Analysed latency variability stemming from processor architecture and helped verify proposed solutions.

System Software Engineer Jul 2015 – Jul 2017

- Developed device drivers to manage memory bandwidth allocations and participated in kernel bring-up on Tegra Parker.
- Developed the infrastructure to deploy Linux Kernel on the full-chip simulation platform for Tegra Xavier.
- Successfully led a cross-organizational effort to integrate the new full-chip simulation platform with a new regression testing infrastructure.
- Mentored an internship project which overhauled the simulator software startup process to create a seamless silicon-like flow.

NVIDIA Beaverton

System Software Intern May 2014 – Aug 2014

- Completed various projects to enhance Tegra full chip simulation environment. As the final project enabled DMA access between simulator and physical IO devices. Snooped kernel requests to the simulated IOMMU to set up address translations via the Linux VFIO framework.

NetApp Bangalore

Member of Technical Staff II, NFS Server Development May 2012 – Jul 2013

- A rich learning experience, specifically in Network File system (NFS) protocol, File Systems, Multi-Processor Programming, Networking, Distributed Systems, High Availability Clustering Systems, development in Unix environment, Security protocols (Kerberos, SSL), Debugging and Software Development Cycle.

Member of Technical Staff I, NFS Server Sustenance Jun 2011 – Apr 2012

- As part of a customer response team, helped ensure timely resolution of customer issues in NetApp's Network File System (NFS) server.
- In a team of 3, conceptualized an invention optimizing stale mount points handling within NFS server implementations, resulting in a monetary award.

Member of Technical Staff I, CIFS Server Quality Assurance Jul 2010 – Jun 2011

- Ensure high quality of NetApp's Common Internet File System (CIFS) server. Helped verify multiple releases, train outsource partners and mentor interns.

Broadcom Bangalore

Intern, Bluetooth Firmware Team Jan 2010 – Jun 2010

- Developed a Perl based Bluetooth device emulator, capable of emulating different Bluetooth Human Interface Devices.

Teaching

Department of Computer Science, University of Illinois at Urbana-Champaign Urbana

Graduate Teaching Assistant Jan 2020 – May 2020

- Conducted labs and initiated efforts to modernize Embedded System Lab projects. A unique challenge was the switch to remote working due to COVID-19 shutdowns.

Department of Physics, University of Wisconsin-Madison Urbana

Graduate Teaching Assistant Aug 2013 – May 2014

- Conducted labs, tutorials and consultations. Helped develop a new instruction format which focused on inculcating intuition and visualization of classical mechanics.

Awards

2020 Best Paper, IEEE Real-Time Systems Symposium

2017 Saburo Muroga Endowed Fellowship, University of Illinois Urbana-Champaign

2015 Graduate Academic Achievement Award, ISS, University of Wisconsin-Madison

2015 Best Student Paper, International Conference on VLSI Design

Publications

Synergistic Perception and Control Simplex for Verifiable Safe Vertical Landing
Ayoosh Bansal, Yang Zhao, James Zhu, Sheng Cheng, Yuliang Gu, Hyung Jin Yoon, Hunmin Kim, Naira Hovakimyan, Lui R Sha
AIAA SCITECH 2024 Forum, 2024

Taming Algorithmic Priority Inversion in Mission-Critical Perception Pipelines
Shengzhong Liu, Shuochao Yao, Xinzhe Fu, Rohan Tabish, Simon Yu, **Ayoosh Bansal**, Heechul Yun, Lui Sha, Tarek Abdelzaher
Communications of the ACM 67.2 (2024) pp. 110–117. ACM New York, NY, USA, 2024

System Auditing for Real-Time Systems
Ayoosh Bansal, Anant Kandikuppa, Monowar Hasan, Chien-Ying Chen, Adam Bates, Sibin Mohan
ACM Transactions on Privacy and Security (2023). ACM, 2023

SchedGuard++: Protecting against Schedule Leaks Using Linux Containers on Multi-Core Processors
Jiyang Chen, Tomasz Kloda, Rohan Tabish, **Ayoosh Bansal**, Chien-Ying Chen, Bo Liu, Sibin Mohan, Marco Caccamo, Lui Sha
ACM Transactions on Cyber-Physical Systems 7.1 (2023) pp. 1–25. ACM New York, NY, 2023

Towards Efficient Auditing for Real-Time Systems
Ayoosh Bansal, Anant Kandikuppa, Chien-Ying Chen, Monowar Hasan, Adam Bates, Sibin Mohan
European Symposium on Research in Computer Security, 2022

Verifiable obstacle detection
Ayoosh Bansal, Hunmin Kim, Simon Yu, Bo Li, Naira Hovakimyan, Marco Caccamo, Lui Sha
2022 IEEE 33rd International Symposium on Software Reliability Engineering (ISSRE), 2022

Risk Ranked Recall: Collision Safety Metric for Object Detection Systems in Autonomous Vehicles
Ayoosh Bansal, Jayati Singh, Micaela Verucchi, Marco Caccamo, Lui Sha
2021 10th Mediterranean Conference on Embedded Computing (MECO), 2021

SchedGuard: Protecting against Schedule Leaks Using Linux Containers
Jiyang Chen, Tomasz Kloda, **Ayoosh Bansal**, Rohan Tabish, Chien-Ying Chen, Bo Liu, Sibin Mohan, Marco Caccamo, Lui Sha
27th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'21), 2021

Reconciling predictability and coherent caching
Ayoosh Bansal, Jayati Singh, Yifan Hao, Jen-Yang Wen, Renato Mancuso, Marco Caccamo
2020 9th Mediterranean Conference on Embedded Computing (MECO), 2020

On removing algorithmic priority inversion from mission-critical machine inference pipelines
Shengzhong Liu, Shuochao Yao, Xinzhe Fu, Rohan Tabish, Simon Yu, **Ayoosh Bansal**, Heechul Yun, Lui Sha, Tarek Abdelzaher
2020 IEEE Real-Time Systems Symposium (RTSS), 2020

Evaluating the memory subsystem of a configurable heterogeneous mpsoc
Ayoosh Bansal, Rohan Tabish, Giovani Gracioli, Renato Mancuso, Rodolfo Pellizzoni, Marco Caccamo
Workshop on Operating Systems Platforms for Embedded Real-Time Applications (OSPERT), 2018

Thermal extension of the total bandwidth server
Rehan Ahmed, **Ayoosh Bansal**, Bhuvana Kakunoori, Parameswaran Ramanathan, Kewal K Saluja
2015 28th International Conference on VLSI Design, 2015

Work In Progress

Perception Simplex: Verifiable Collision Avoidance in Autonomous Vehicles Amidst Obstacle Detection Faults
Ayoosh Bansal, Hunmin Kim, Simon Yu, Bo Li, Naira Hovakimyan, Marco Caccamo, Lui Sha

SITL Evaluation and Benchmarking framework for Autonomous Air Taxis
Ayoosh Bansal, Yang Zhao, Chejian Xu, Oswin So, Sheng Cheng, Chuchu Fan, Bo Li, Naira Hovakimyan, Lui Sha

Synergistic Simplex: Cooperative Redundancy for Safety-Critical Cyber-Physical Systems
Ayoosh Bansal, James Zhu, Hunmin Kim, Lui Sha

Verifiable Safe Vertical Landing in presence of 6D Disturbances and Pose Dynamics
Yang Zhao, **Ayoosh Bansal**, James Zhu, Sheng Cheng, Yuliang Gu, Hyung Jin Yoon, Hunmin Kim, Naira Hovakimyan, Lui R Sha

Presentations

Jan 2024 Synergistic Perception and Control Simplex for Verifiable Safe Vertical Landing, AIAA SCITECH 2024 Forum
Nov 2023 Certifiably Safe and Robust Perception for Learning-enabled Autonomy, AVIATE Center NASA ULI Annual Review
Nov 2022 Verifiable obstacle detection, IEEE 33rd International Symposium on Software Reliability Engineering (ISSRE)
Jan 2015 Thermal extension of the total bandwidth server, 28th International Conference on VLSI Design