# Ayoosh Bansal

ayooshbansal@gmail.com | ayooshbansal.com | linkedin.com/in/ayooshbansal/ | Ayoosh Bansal

## Education

**University of Illinois Urbana-Champaign**

PhD in Computer Science, Advised by Prof. Lui Sha, GPA 4/4 — Aug 2017 - Aug 2024

Dissertation Title : Safe and Secure Autonomous Driving

Research Topics : System Architecture, Autonomous Vehicle Safety, Real-Time Systems, Computer Architecture

**University of Wisconsin-Madison**

Master of Science in Electrical Engineering, GPA 4/4 — Sep 2013 - May 2015

**Birla Institute of Technology and Science Pilani, India**

Bachelor of Engineering Electrical and Electronics, CGPA 8.6/10 — Aug 2006 - Jul 2010

## Experience

**Cyber Physical Systems Integration Lab, UIUC** — Urbana, Illinois, USA

*Postdoctoral Research Associate* — Oct 2024 – Present

- Designing *Synergistic Simplex* system architecture that harnesses cooperation among safety- and mission-critical elements to enhance the safety and performance of autonomous ground and aerial vehicles.
- As part of a collaborative effort, including industrial partners from NASA, designing and developing AirTaxiSim, a photorealistic software-in-the-loop simulation framework for autonomous air taxis.

*Graduate Research Assistant* — Aug 2017 – Aug 2024

- Led multiple research projects, architecting system solutions for enhancing functional safety, bolstering system security, and refining temporal predictability in cyber-physical and real-time systems, with a focus on autonomous ground and aerial vehicles.
- Introduced a new memory type, *Inner Non-Cacheable, Outer Cacheable*, empowering real-time applications to bypass cache coherence mechanisms and mitigate memory access latency variability, selectively for shared data, with no impact on private data. Prototype implementation on Linux Kernel and Gem5 simulator, yielded 52% reduced worst-case latency and negligible impact on performance.
- Designed a scratchpad based cooperative execution model between processor cores and hardware accelerators, achieving similar energy and latency efficiency as monolithic fixed function hardware accelerators, while supporting flexible functions.
- Pioneered verifiable perception safety in autonomous ground vehicles by developing *Perception Simplex*, a system architecture that provides verifiable obstacle detection and deterministic collision avoidance within the operational design domain. The safety guarantees were proven analytically and validated using open-source industrial simulation frameworks.
- Adapted *Perception Simplex* to aerial vehicles, while improving its performance by closely integrating low-level control to dynamically confirm the control capabilities of the system, rather than assume static worst-case.
- Recognizing the lack of context-aware metrics for object detection in autonomous driving, created *Risk Ranked Recall*. This metric differentiates between objects based on their potential safety impacts.
- To bring security auditing to real-time systems, created *Ellipsis*. Harnessing the inherent predictability of behaviors in real-time applications, *Ellipsis* optimizes Linux Audit for real-time applications. *Ellipsis* all but eliminates the possibility of audit event loss during typical operation and significantly curtails auditing data volume (> 90%) while preserving security-relevant information.
- Helped develop an input prioritization scheme for object detection neural networks overcoming an inherent priority inversion and a security-aware task scheduling for real-time applications, minimizing the impacts of posterior schedule based class of attacks.

**NVIDIA** — Santa Clara

*Automotive System Software Intern* — May 2020 – Aug 2020

- Developed a hypervisor-level latency analysis system aimed at optimizing applications with stringent latency requirements.

*Automotive System Software Intern* — Jun 2018 – Aug 2018

- Analysed latency variability stemming from processor architecture and helped verify proposed solutions.

*System Software Engineer* — Jul 2015 – Jul 2017

- Developed device drivers to manage memory bandwidth allocations and participated in kernel bring-up on Tegra Parker.
- Developed the infrastructure to deploy Linux Kernel on the full-chip simulation platform for Tegra Xavier.
- Successfully led a cross-organizational effort to integrate the new full-chip simulation platform with a new regression testing infrastructure.
- Mentored an internship project which overhauled the simulator software startup process to create a seamless silicon-like flow.

**NetApp** — Bangalore

*Member of Technical Staff* — Jul 2010 – Jul 2013

- Progressed through roles in CIFS server quality assurance, NFS server maintenance, and finally NFS server development.
- Resolved diverse customer issues and escalations, mitigating active disruptions. Conducted SSH CVE applicability analysis.
- Conceptualized an invention optimizing stale mount points handling within NFS server implementations, resulting in a monetary award.

## Skills

C, Python, C++, Assembly, Linux Kernel Development, Git, Gem5, Perl, Verilog, Cyber-RT, ROS, Gem5-Aladdin, LLVM, Xilinx Vivado.

Work Authorization: Eligible to work in USA through Optional Practical Training